IN THE SPECIFICATION:

Please add the following at page 1, before the Background of the Invention section of the above-referenced application:

CROSS-REFERENCE TO RELATED APPLICATIONS

This patent application is a divisional application of U.S. Application Serial No. 09/474,662, filed on December 29, 1999, and may benefit from the priority thereof.

Please replace the paragraph starting on line 13 as follows:

Printed circuit boards (PCBs) are widely used in the electronics and computer industries to mechanically and electrically couple individual components. A "motherboards" in a personal computer (PC), used to mount, and connect, a central processing unit (CPU) with other associated components is but one common example of a PCB. Generally, a PCB comprises a number of layers through which electrical signals may be routed, separated by dielectric layers. The layers for routing electrical signals may contain multiple (conducting) traces, each electrically isolated, or the entire layer may be electrically conductive. Conductive layers may be used to efficiently provide access to a particular voltage level, or voltage plane, over the entire area of the PCB. PCBs with one ~~on~~ or more power planes, at voltages such as V_{dd}, and one or more ground planes are relatively common.

Please replace the last paragraph on page 1 as follows:

One design choice in routing signals within a PCB, is between routing on the top layer (microstrip routing) or routing in one of the inner layers (stripline routing). Microstrip routing typically provides faster signal speeds or "flight times" ~~and microstrip routing,~~ at the expense of requiring more complete connections to the routing traces. Signal speeds of 153 ps/in for microstrip routing and 170 ps/in for stripline routing are typical. An advantage of stripline ~~stipline~~ routing is that such a routing makes it easier to electrically isolate the signals using isolation lines and ground planes.

Please replace the first full paragraph on page 2 as follows:

The design of a trace, or conductor for a particular signal path, depends on many factors. Two important factors being the locations of the points to be connected and the required impedance of the trace. The required impedance will typically be set by the components connected by the trace, with the actual impedance a function of the inductance and capacitance of the particular trace design. Eventually, the length, width, and geometry of the trace are defined for an acceptable signal routing scheme. However, there are combinations of clock speeds and signal values that degrade the quality of signal transmissions for a given signal routing scheme. Resonances ~~Resources~~ within a PCB may occur a signal on a single signal path, although isolated from other signals on the PCB, oscillates at, or near an integer multiple of signal transmit time. Such resonance may seriously degrade the performance of the PCB.

On page 3, line 19, replace the sentence as follows:

Figure 3 is a cross section through ~~of~~ a PCB showing the multiple layers.

On page 3, line 21, replace the sentence as follows:

Figure 4A-4B depicts two layouts of a signal trace of ~~or~~ a PCB.

On page 4, 3rd paragraph, replace the paragraph as follows:

In the design of traces 2 for high speed electronic devices, such as, but[,] not limited to, PCB 4, great care is often taken to avoid interference with signals carried by traces 2. Figure 2, shows one such design that may be used to shield a signal carried by trace 2. It~~, it~~ is an enlarged view of trace 2 on a layer of PCB 4. Trace 2 is a 18 mil wide conductor, that is located between two 5 mil wide isolation lines 8. Isolation lines 8 are typically conductive and are preferably grounded to a single common ground. In a PCB 4, each of the signal traces 2 may be surrounded on the particular "horizontal" layer within PCB 4, by insulators 6 and isolation lines 8. In addition, signal trace 2 may be shielded vertically within PCB 4. Turning now to Figure 3, a

cross section through a PCB, a particular layer 10 with traces 2, such as shown in Figure 1, makes up but one horizontal layer with a PCB 14. With such a design, trace 2 is surrounded both horizontally and vertically with a dielectric and a ground in order to isolate trace 2 and to minimize the effects of other signals on the one carried by trace 2. There are, however, situations where such isolation alone is not effective, resulting in poor device performance, such as single bit errors. These problems and some solutions to them will be further elaborated below.

On page 5, replace the first full paragraph with the following:

One use of PCBs 4 is to allow standard configurations, such as a standard connect pin layout on a device, while using dissimilar component level devices to make up the device. A common example, known to those of ordinary skill in the art, would be single inline memory modules (SIMMs) such as a 72-pin SIMM specified by the Joint Electronic Device Electroneering Council (JEDEC). Although many memory components, of varying sizes, may be used by various manufacturers ~~manufactures~~, the resulting device will "plug in" to a standard 72-pin SIMM socket. Thus, the standardization of a particular PCB 4 layout, such as size and connection geometry, can be valuable. This is the case even though such a standard layout may not be "optimal" for each particular embodiment in design of performance.

On page 7, replace the second paragraph as follows:

Preferably, the transit times of signals would differ from multiples of the period of the data transfer rate. One way to achieve this result, without altering the clock speed, is to change the lengths of traces 2 slightly to "detune" PCB 4. Figures 4A and 4B show one embodiment of lengthening traces 2. However, such lengthening of traces 2 does not directly effect resonance problems within a ground plane. In one case, detuning traces 2 still left the ground plane with a resonance caused flunctuation of approximately 100 mV. Eliminating such a fluctuation in the ~~grand~~ ground plane increases the signal-to-noise (S/N) ratio, which tends to decrease data transmission errors.

On page 7, replace the second full paragraph as follows:

Electrical signals to and from any device typically require two conductors; typically a trace and a ground plane in PCB 4. Since a ground plane is typically a conductive layer of PCB 4, not individual traces 2, increasing the signal transit times through the ground plane requires different techniques than the lengthening used for traces 2. An embodiment of the present invention uses cuts in the conductive layer of a ground plane to reduce resonance and improve overall signal performance. Preferably, the cuts in a ground plane are coordinated with the laying out and lengthening of traces 2.

On page 7, replace the third full paragraph as follows:

Figure 5 illustrates a PCB 4 with cuts made to a ground plane, in accordance with an embodiment of the present invention. Traces 2 have been lengthened, similar to that shown in Figure 4B. The locations of ground plane cuts 16 are preferably coordinated with the locations of traces 2. Although only a single trace 2 layout is shown in Figure 5, the location of all traces 2 and ground plane cuts 16 on ~~or~~ PCB 4 are preferably coordinated such that cuts 16 terminate at least 10 miles from a ~~an~~ trace 2. In one embodiment of the present invention, the locations of ground ~~grand~~ plane cuts 16are similar in each ground ~~grand~~ plane layer within PCB 4. That is, cuts 16 are vertically aligned.

On page 8, replace the second full paragraph as follows:

Figure 6 illustrates such a zipper cut pattern. Along the axis of cut 16, a series of approximately 10 mil long by 5 mil wide holes are created in the ground plane at spacings of ~~a~~ 20 mil, ~~spacings~~ center-to-center. The effect of a zipper cut pattern is a smaller decrease in signal transit times through a ground plane than a continuous cut 16 at the same location.